REMARKS

Claims 1 to 3, 5, 6, 8, 10, 14 and 15 were rejected under 35 U.S.C.103(a) as being unpatentable over Birleson (U.S. 6,163,684) in view of Fujii (U.S. 6,396,330B1). The rejection is again respectfully traversed.

To begin with, the subject application refers to a frequency generator whereas Birleson down converts a received signal to a 45 MHZ IF that a receiver converts to a television signal. It follows that the purpose alone of the subject application is entirely different from that of Birleson. The subject application is a transmitter chain to generate the 55 to 800 MHZ signal and provides an up-conversion of a single oscillator reference to a wide range of output frequencies. Furthermore, the improvement in the subject application is not just for multiple PLLs, but rather for the manner in which the PLLs are connected. The unique connection of the subject circuit provides superior phase noise performance and frequency range over other ways of connecting multiple PLLs.

In this regard, all of the claims require, in addition to other features, that the input to the fine tune PLL and to the course loop PLL be the same input signal and be coupled to the same input terminal. No such feature is anywhere taught or suggested by Birleson, Fujii and any proper combination of these references.

With reference to claim 1, in addition to the arguments previously presented, which are repeated, this claim specifically requires an input terminal for receiving an input reference signal having a frequency f_R; with both, a fine tune phase locked loop coupled to the input terminal and driven by the input reference signal to output a fine tune signal having a frequency $f_R \cdot P$, where P is an integer and a coarse tune phase locked loop coupled to the input terminal and driven by the input reference signal to output a coarse tune signal having a frequency $f_R \cdot A$, where A is an integer. No such arrangement is taught or suggested by Birleson, Fujii or any proper combination of these references.

Claim 1 further requires a translation phase locked loop having a unity multiplication factor driven by the fine tune signal No such feature is taught or suggested by Birleson, Fujii or any proper combination of these references.

Claim 1 still further requires that the translation loop contain a Gilbert cell double balanced mixer coupled between the coarse tune and the translation phase locked loops, the Gilbert cell mixer combining the coarse tune signal and a divided down output signal of the fine tune phase locked loop and coupling the mixed signal into the translation phase locked loop to generate an output signal with a frequency which is proportional to the linear sum of the coarse tune signal and the fine tune signal, the low multiplication factor and high bandwidth of the coarse tune loop and the unity multiplication factor of the translation loop reducing the phase noise of the frequency synthesizer. No such feature is taught or suggested by Birleson, Fujii or any proper combination of these references.

Furthermore, with respect to Birleson, none of the PLL in Birleson are denoted to be fine tune, course tune or translation loops as required by the claims. It appears that the examiner has arbitrarily chosen these designations whereas no proper basis therefore appears to exist.

Claims 2, 3, 5, 6, 8 and 10 depend from claim 1 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 1.

The features discussed above with reference to claim 1 are found in claim 14 in method format.

Claim 15 depends from claim 14 and therefore defines patentably over the applied references for at least the reasons presented above with reference to claim 1.

Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable ove Birleson in view of Fujii further in view of Bezzam et al. (U.S. 6,115,586). The rejection is respectfully traversed.

Claim 4 depends from claim 1 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 1 since Bezzam et al. fails to overcome the deficiencies in Birleson and Fujii as discussed above.

Claim 7 further limits claim 1 by requiring the frequency synthesizer of claim 1, wherein the translation phase locked loop includes a low pass filter coupled to receive the mixed signal output of the Gilbert cell double balanced mixer and to produce a filtered output signal, a phase detector coupled to receive the divided down fine tune signal and the filtered output signal of the low pass filter and to output a phase detection signal, a loop filter coupled to receive the phase detection signal and to output a tune voltage, a voltage controlled oscillator coupled to receive the tune voltage output of the loop filter and generate a signal frequency proportion to the tune voltage and a Gilbert cell double balanced mixer coupled between the coarse tune and the translation phase locked loops, the Gilbert cell mixer combining the coarse tune signal and the divided down output signal of the fine tune phase locked loop and couples the mixed signal into the low pass filter of the translation loop, generating an output signal with a frequency which is proportional to the linear sum of the coarse tune signal and the fine tune signal. No such combination is taught or suggested by the applied references.

Claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Birleson in view of Fujii further in view of Hirata et al. (U.S. 5,353,311). The rejection is respectfully traversed.

Claim 11 depends from claim 3 and therefore defines patentably over the applied references for at least the reasons presented above with reference to claim 3. Furthermore, no such combination is taught or suggested by the applied references since there is no teaching or suggestion to combine the references in the manner applied by the examiner.

The allowability of claims 7, 9, 12, 13 and 16 when written in independent form is noted and appreciated.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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